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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,099	07/18/2003	Ken Gary Pomaranski	200310409-1	2888

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EXAMINER	
LE, DIEU MINH T	
ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,099	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *101205 & 020106*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is response to the communication filed on 12/30/03 in application 10/622,780.

2. Claims 1-21 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vosbury (U.S. Patent 5,138,708) in view of Vrba et al. (U.S. Patent 5,845,060 hereafter referred to as Vrba).

As per claim 1:

Vosbury explicitly teach the invention. Vosbury teaches:
- microprocessor for targeted fault-tolerant computing, the microprocessor [abstract, fig. 1-3, col. 1, lines 1-12] comprising:
- decode circuitry configured to decode a fault-tolerant version of an instruction [abstract, col. 1, lines 60 through col. 2, lines 9; col. 3, lines 5-25];
- execution circuitry configured to execute the fault-tolerant version of the instruction with redundancy checking [abstract, col. 1, lines 60 through col. 2, lines 9; col. 3, lines 5-25].

Vosbury does not explicitly teach:
- a non-fault-tolerant version of the instruction.

However, Vosbury does disclose capability of:
- A highly fault-tolerant processing system comprising first and second CPU for executing instructions [abstract, col. 1, lines 60 through col. 2, lines 9.] comprising capabilities of:

- ***a uniprocessing (i.e., non-fault-tolerant)as well as a multiprocessing (i.e., fault-tolerant) processes in supporting the microprocessing fault-tolerant computing system*** [col. 4, lines 40-63]..

In addition, Vrba does explicitly disclose:

- A fault tolerant computing system comprising multi-processors for executing instructions [abstract, fig. 4, col. 2, lines 20-26] comprising
- ***fault-tolerant and non-fault-tolerant processors used to executing instructions in supporting the fault-tolerant computing system*** [col. 12, lines 14-30].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize that the Vosbury's ***a uniprocessing (i.e., non-fault-tolerant)as well as a multiprocessing (i.e., fault-tolerant) processes in supporting the microprocessing fault-tolerant computing system*** capability does perform such Applicant's non-fault-tolerant version of the instruction limitation. This is because Vosbury clearly applied these executing instruction for testing configuration, comparison, simulation, evaluation, performance in determining whether the system functioned properly; second, by applying the capability of ***fault-tolerant and non-fault-tolerant processors used to executing instructions in supporting the fault-tolerant computing system*** as taught by Vrba in conjunction with the highly fault-tolerant processing system comprising first and second CPU for executing instructions as taught by Vosbury, the computer/communication data processing system, more specifically the fault-tolerant computing system, can enhance its operation

performance, more specifically to ensuring the error thoroughly detected and corrected via signature and/or instruction comparison process.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the fault-tolerant computer system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data displaying, data *reliability*, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 2 and 5:

Vosbury further explicitly teaches:

- a first processing unit configured to receive operand data, execute an operation associated with the instruction; and generate a first result [abstract, fig. 1-3, col. 2, lines 25-58] comprising:
- a second processing unit configured to receive the operand data; execute the operation, and generate a second result [, fig. 1-3, col. 2, lines 25-58];
- a comparator configured to compare the first and second results [, fig. 1-3, col. 2, lines 25-58].
- a register file configured to provide both the first and second processing units with the operand data [col. 1, lines 60 through col. 2, lines 8].

In addition, Vrba does explicitly disclose:

- A fault tolerant computing system comprising multi-processors for executing instructions [abstract, fig. 4, col. 2, lines 20-26] comprising
- fault-tolerant and non-fault-tolerant processors used to executing instructions in supporting the fault-tolerant computing system [col. 12, lines 14-30].
- ***multi-processors' speed and outputs comparison in supporting the fault-tolerant computing system [col. 2, lines 43-67 and col. 3, lines 35-47].***
- a register file configured to provide both the first and second processing units with the operand data [col. 8, lines 20-42].

As per claims 3-4:

Vosbury explicitly teach the invention. Vosbury teaches:
- microprocessor for targeted fault-tolerant computing, the microprocessor [abstract, fig. 1-3, col. 1, lines 1-12] comprising:
- ***a uniprocessing (i.e., non-fault-tolerant)as well as a multiprocessing (i.e., fault-tolerant) processes in supporting the microprocessing fault-tolerant computing system*** [col. 4, lines 40-63].

Vosbury does not explicitly teach:
- comparison of results by comparator up to a maximum N times until a match occurs and a machine check is performed if first and second results never match.

However, Vosbury does disclose capability of:

- A highly fault-tolerant processing system comprising first and second CPU for executing instructions [abstract, col. 1, lines 60 through col. 2, lines 9.] comprising capabilities of:
- ***a comparison in a number of times (i.e., N times) and if operation continuously unsuccessful then the system goes into diagnostics mode (i.e., machine check)*** [col. 4, lines 46 through col. 5, lines 17].

In addition, Vrba does explicitly disclose:
- A fault tolerant computing system comprising multi-processors for executing instructions [abstract, fig. 4, col. 2, lines 20-26] comprising
- fault-tolerant and non-fault-tolerant processors used to executing instructions in supporting the fault-tolerant computing system [col. 12, lines 14-30].
- ***decision results based on multiple comparison processes applied in fault-tolerant computing system*** [col. 12, lines 30-64].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize that the Vosbury's ***a comparison in a number of times (i.e., N times) and if operation continuously unsuccessful then the system goes into diagnostics mode (i.e., machine check)*** capability does perform such Applicant's fault and non-fault-tolerant version of the instruction limitation. This is because Vosbury clearly applied repeat and retry comparison (i.e., N times) functionality for testing configuration, comparison, simulation, evaluation, performance in determining whether the

system functioned properly; second, by applying the capability of ***decision results based on multiple comparison processes applied in fault-tolerant computing system*** as taught by Vrba in conjunction with the highly fault-tolerant processing system comprising first and second CPU for executing instructions as taught by Vosbury, the computer/communication data processing system, more specifically the fault-tolerant computing system, can enhance its operation performance, more specifically to ensuring the error thoroughly detected and corrected via signature and/or instruction comparison process for the same reasons set forth as described in claim 1, **supra.**

As per claims 6-13, and 21:

Due to the similarity of claims 6-13, and 21 to claims 1-5 except for a ***method*** for targeted fault-tolerant computing in a CPU comprising decoding a first op code corresponding to a fault-tolerant version of an instruction, a second op code corresponding to a non-fault-tolerant version of an instruction, executing first op code and second op code, respectively etc…; instead of ***the microprocessor*** for targeted fault-tolerant computing comprising a decoding circuit for decoding a fault-tolerant version of instruction, executing circuit for executing the fault tolerant version of the instruction, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-5. **In addition, all of the limitations have been noted in the rejection as per claims 1-5, such as *op code, arithmetic function (i.e., Vosbury, EXCLUSIVE OR LOGIC FUNCTION*** [fig. 1-3, col. 3, lines 3-25].

As per claims 14-15:

Due to the similarity of claims 14-15 to claims 1-5 except for ***a computing apparatus*** for targeted fault-tolerant computing comprising a decoding MEANS for decoding a first op code corresponding to a fault-tolerant version of instruction, a redundant and non-redundant MEANS for executing first op code and second op code, respectively, etc… instead of ***the microprocessor*** for targeted fault-tolerant computing comprising a decoding circuit for decoding a fault-tolerant version of instruction, executing circuit for executing the fault tolerant version of the instruction, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-5. **In addition, all of the limitations have been noted in the rejection as per claims 1-5,** such as ***redundancy and checking for duplicate data*** [Vrba, col. 2, lines 27-43 and col. 3, lines 25-33].

As per claims 16-20:

These claims are the same as per claims 1-5. The only minor different is that these claims are directed to a **computer program product** instead of ***the microprocessor*** for targeted fault-tolerant computing comprising a decoding circuit for decoding a fault-tolerant version of instruction, executing circuit for executing the fault tolerant version of the instruction, etc… as described in claims 1-5. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that a computer program product is a necessary item for such failure detection (i.e., fault-tolerant) system. Since the computer failure detecting processing system obviously needs a means for instruction or code means resided within the computer program product for

performing the instruction identifying, comparing, and processing including the failure detection and correction (e.g., matching measure). **Therefore, these claims are also rejected under the same rationale applied against claims 1-5.**

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER
ART UNIT 2114

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